Amendments to the Claims

Please cancel Claims 1-17 without prejudice. Applicant reserves the right to refile them in a continuation application. Please add new Claims 18-69. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1-17. (canceled)

18. (new) A synchronous memory comprising:

a clock input signal; and

a delay locked loop (DLL) having an adjustable delay line for generating a driving clock signal from the clock input signal, the DLL being enabled and disabled by external control.

19. (new) Synchronous memory as claimed in claim 18 wherein the DLL is disabled during a standby state.

20. (new) Synchronous memory as claimed in claim 18 further comprising a clock buffer coupled to the clock input signal for generating a buffered clock signal, the buffered clock signal being used when the DLL is disabled.

21. (new) Synchronous memory as claimed in claim 18 wherein settings of the delay line are maintained when the DLL is disabled.

22. (new) Synchronous memory as claimed in claim 21 wherein the settings are maintained during power down.

23. (new) Synchronous memory as claimed in claim 21 wherein the settings are maintained during a standby state.

24. (new) Synchronous memory as claimed in claim 18 further comprising a delay comparator coupled to the adjustable delay line for setting the delay though the delay line, the comparator having a first input coupled to the clock input signal and a second input coupled to the driving clock signal.

25. (new) Synchronous memory as claimed in claim 24 further comprising a delay model coupled between the driving clock signal and the delay comparator, the delay model comprising similar elements as the circuit path taken by the clock input signal.

26. (new) Synchronous memory as claimed in claim 18 wherein the adjustable delay line is a tapped delay line.

27. (new) Synchronous memory as claimed in claim 26 wherein taps provide plural outputs of the delay line.

28. (new) Synchronous memory as claimed in claim 27 wherein a comparator in the DLL determines one of the tap outputs that forms the driving clock signal.

29. (new) Synchronous memory as claimed in claim 18 further comprising a data output buffer enabled by the driving clock signal for outputting data to an output terminal.

30. (new) Synchronous memory as claimed in claim 18 wherein the DLL is enabled and disabled by a register bit.

31. (new) Synchronous memory as claimed in claim 18 wherein the DLL is enabled and disabled by register data.

32. (new) Synchronous memory as claimed in claim 18 wherein the DLL is enabled and disabled by a register.

33. (new) A synchronous dynamic random access memory comprising:

a clock input signal; and

a delay locked loop (DLL) having an adjustable delay line for generating a driving clock signal from the clock input signal, the DLL being enabled and disabled by external control.

34. (new) A method of providing a clock to a synchronous memory comprising:

generating a driving clock signal from a clock input signal through a delay locked loop (DLL) having an adjustable delay line; and

using external control, disabling the delay locked loop.

35. (new) The method of claim 34 wherein the DLL is disabled during a standby state.

36. (new) The method of claim 34 further comprising generating a buffered clock signal from the clock input signal and using the buffered clock signal when the DLL is disabled.

37. (new) A method as claimed in claim 34 further comprising maintaining settings of the delay line when the DLL is disabled.

38. (new) The method of claim 37 wherein the settings are maintained during power down.

39. (new) The method of claim 37 wherein the settings are maintained during a standby state.

40. (new) The method of claim 34 further comprising setting the delay through the delay line with a comparator having a first input coupled to the clock input signal and a second input coupled to the driving clock signal.

41. (new) The method of claim 40 wherein the driving clock signal is delayed in a delay

model having similar elements as the circuit path taken by the clock input signal.

42. (new) The method of claim 34 wherein the adjustable delay line is a tapped delay line.

43. (new) The method of claim 42 wherein taps provide plural outputs of the delay line.

44. (new) The method of claim 43 wherein one of the tap outputs is determined by a comparator in the DLL to form the driving clock signal.

45. (new) The method of claim 34 wherein the driving clock signal enables a data output buffer for outputting data to an output terminal.

46. (new) The method of claim 34 wherein the external control sets and resets a register bit to enable and disable the DLL.

47. (new) The method of claim 34 wherein the external control changes register data to enable and disable the DLL.

48. (new) The method of claim 34 wherein the external control controls a register to enable and disable the DLL.

49. (new) A synchronous memory comprising:

means for generating a driving clock signal from a clock input signal through a delay locked loop (DLL) having an adjustable delay line; and

means for disabling the delay locked loop by external control.

50. (new) A synchronous memory comprising:

a clock input signal;

a buffer that receives the clock input signal and provides a buffered clock signal;

a delay locked loop (DLL) that receives the clock input signal and generates a

driving clock signal; and

circuitry that receives the driving clock signal when the DLL is enabled and receives the buffered clock signal when the DLL is disabled.

51. (new) A synchronous memory as claimed in claim 50 further comprising register data that enables or disables the DLL.

52. (new) A synchronous memory as claimed in claim 50 further comprising a register bit that enables or disables the DLL.

53. (new) A synchronous memory as claimed in claim 50 further comprising a register that enables or disables the DLL.

54. (new) A synchronous memory as claimed in claim 50 wherein the DLL further comprises an adjustable delay line and a delay comparator, the delay comparator determining the delay through the adjustable delay line.

55. (new) A synchronous memory as claimed in claim 54 wherein settings of the adjustable delay line are maintained when the DLL is disabled.

56. (new) Synchronous memory as claimed in claim 55 wherein the settings are maintained during power down.

57. (new) Synchronous memory as claimed in claim 55 wherein the settings are maintained during a standby state.

58. (new) A synchronous memory as claimed in claim 50 wherein said circuitry contains a data output buffer enabled by the driving clock signal or buffered clock signal.

59. (new) A synchronous dynamic random access memory comprising:

a clock input signal;

a buffer that receives the clock input signal and provides a buffered clock signal;

a delay locked loop (DLL) that receives the clock input signal and generates a driving clock signal; and

circuitry that receives the driving clock signal when the DLL is enabled and receives the buffered clock signal when the DLL is disabled.

60. (new) A method of providing a clock to a synchronous memory comprising:

generating a driving clock signal with a delay locked loop (DLL);

buffering a clock input signal to provide a buffered clock signal;

providing the driving clock signal to a portion of the synchronous memory when the DLL is enabled; and

providing the buffered clock signal to said portion of the synchronous memory when the DLL is disabled.

61. (new) The method of claim 60 further comprising providing register data to enable or disable the DLL.

62. (new) The method of claim 60 further comprising providing a register bit to enable or disable the DLL.

63. (new) The method of claim 60 further comprising providing a register to enable or disable the DLL.

64. (new) The method of claim 60, wherein the DLL has an adjustable delay line and a delay comparator, the delay comparator determining the delay through the adjustable delay line.

65. (new) The method of claim 64 further comprising the step of maintaining settings of the adjustable delay line when the DLL is disabled.

66. (new) The method of claim 65 wherein the settings are maintained during power down.

67. (new) The method of claim 65 wherein the settings are maintained during a standby state.

68. (new) The method of claim 60 wherein said portion of the synchronous memory contains a data output buffer enabled by the driving clock signal or buffered clock signal.

69. (new) A synchronous memory comprising:

means for generating a driving clock signal with a delay locked loop (DLL);

means for buffering a clock input signal to provide a buffered clock signal;

means for providing the driving clock signal to a portion of the synchronous memory when the DLL is enabled; and

means for providing the buffered clock signal to said portion of the synchronous memory when the DLL is disabled.